

What is claimed is:

*Sub 26*

1. A controller of a system connected to a memory, which stores firmware, for operating in accordance with the  
5 firmware stored in the memory, the controller comprises:  
a data processing circuit that performs predetermined processing on data and generates processed data;  
a write wire connected to the memory; and  
a terminal for used in the output of the data processed  
10 by the data processing circuit and/or the provision of the data to the data processing circuit, wherein the controller connects the write wire and the terminal to write the firmware to the memory.

15 2. A controller of a system that operates in accordance with firmware stored in a firmware storing memory, the controller comprises;

a first terminal for receiving and providing data between the controller and an external device;

20 a data processing circuit for performing predetermined processing on the data to be provided to and received from the external device via the first terminal; and

a firmware write wire connected to the firmware storing memory, wherein the control circuit selectively connects the  
25 first terminal and one of the data processing circuit and the firmware write wire.

3. The controller of claim 2, further comprising a selector connected to the data processing circuit and the  
30 firmware write wire for selectively connecting the first terminal and one of the data processing circuit and the firmware write wire in response to a switching signal.

4. The controller of claim 3, further comprising a  
35 second terminal for providing the switch signal to the

selector, wherein the selector connects the data processing circuit and the first terminal when the second terminal is grounded.

5           5. The controller of claim 3, wherein the selector further connects the firmware write wire and the first terminal when the switching signal is active.

10           6. A data processing system connected to an external device via a connector for receiving and providing data between the external device, the system comprising:

          a memory for storing firmware; and

15           a microcomputer connected to the memory for operating in accordance with the firmware stored in the memory, wherein the firmware is written to the memory by directly connecting the memory and the connector.

20           7. The data processing system of claim 6, wherein the data processing system selectively switches the firmware write operation and the reception and provision of the data in response to a switching signal.

25           8. A data processing system connected to an external device via a connector for receiving and providing data between the external device, the system comprising:

          a memory for storing firmware;

          a microcomputer connected to the memory for performing control operation in accordance with the firmware stored in the memory;

30           a data processing circuit connected to the microcomputer for performing predetermined processing on data to be provided to and received from the external device in accordance with the control of the microcomputer; and

35           a selector connected to the data processing circuit and the memory for selectively connecting the connector and one

of the data processing circuit and the memory, wherein the firmware is written to the memory via the connector when the selector connects the connector and the memory.

5           9. In the data processing system of claim 8, wherein the selector switches connection in response to a switching signal, and the selector connects the connector and the data processing circuit when the switching signal is inactive.

10           10. The data processing system of claim 9, further comprising a terminal for providing the switching signal to the selector, wherein the selector connects the connector and the data processing circuit when the terminal is grounded.

15           11. The data processing system of claim 9, wherein the selector further connects the connector and the memory when the switching signal is active.

20           12. The data processing system of claim 8, wherein the connector includes a plurality of the terminals, and the system further comprises a plurality of firmware write wires for connecting the memory and the selector, wherein the number of the plurality of the terminals is larger than the number of the plurality of the firmware write wires.

25           13. The data processing system of claim 8, wherein the memory, the data processing circuit and the selector are mounted on a single LSI.

30           14. The data processing system of claim 8, wherein the memory, the microcomputer, the data processing circuit, and the selector are mounted on a single LSI.